## **IN THE SPECIFICATION**

Please amend the paragraph at page 4, lines 10-25, as follows:

According to an aspect of the present invention, there is provided a magnetic memory device comprising a first conductive layer; a second conductive layer formed above the first conductive layer and arranged substantially perpendicular to the first conductive layer; a plurality of magneto-resistance effect elements formed between the first and second conductive layers, arranged in the lengthwise direction of the first conductive layer and containing free layers whose spin directions are controlled to be reversed by a resultant magnetic field caused by the first and second conductive layers; and a magnetic layer inserted between the first conductive layer and the magneto-resistance effect elements, including a soft magnetic body, and causing magnetic interaction with respect to the free layers of the magneto-resistance effect elements.

Please insert a new paragraph at page 4, between lines 25 and 26, as follows:

According to another aspect of the present invention, there is provided a magnetic memory device comprising: a first conductive layer; a second conductive layer formed above the first conductive layer and arranged substantially perpendicular to the first conductive layer; and a plurality of magneto-resistance effect elements formed between the first and second conductive layers, arranged in the lengthwise direction of the first conductive layer and containing free layers whose spin directions are controlled to be reversed by a resultant magnetic field caused by the first and second conductive layers, where the first conductive layer is formed of a soft magnetic body which causes magnetic interaction with respect to the free layers of the magneto-resistance effect elements, and each of the magneto-resistance effect elements includes a tunnel barrier layer disposed on the free layer, a pin layer disposed

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on the tunnel barrier layer, and a fixing layer disposed on the pin layer and fixing the spin direction of the pin layer.